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**BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI**

**WORK INTEGRATED LEARNING PROGRAMMES**

**COURSE HANDOUT**

**Part A: Content Design**

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| **Course Title** | Computer Organization and Software Systems |
| **Course No(s)** | SS ZG516 |
| **Credit Units** | 5 (1 + 2 + 2)  Unit split between Class Hours + Lab/Design/Fieldwork + Student preparation respectively; each unit translates to 32 hours |
| **Course Author** | Lucy J Gudino / Chandra Shekhar |
| **Version No** | 1.0 |
| **Date** |  |

**Course Objectives**

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| **No** | **Course Objective** |
| **CO1** | Introduce students to systems aspects ( i.e. Computer Organization and Operating Systems) involved in software development |
| **CO2** | Equip the student to understand the computer architectural and operating systems related issues that affect the performance and nature of a software |
| **CO3** | To prepare students to be in a position to evaluate/correlate high level software performance based on its system level features (i.e. architectural and operating systems) |

**Text Book(s)**

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| T1 | Stallings William, Computer Organization & Architecture, Pearson Education, 9th Ed. 2013 |
| T2 | A Silberschatz, Abraham and others, Operating Systems Concepts, Wiley Student Edition, 8th Edition |

**Reference Book(s) & other resources**

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| R1 | Patterson, David A & J L Hennenssy, Computer Organisation & Design, Elsevier, 4th Ed., 2009. |
| R2 | Ghosal, Computer Organization and Architecture: From 8085 to core2Duo & Beyond (For JNTUK), Pearson Education, 2011 (Pearson Online) |
| R3 | Tanenbaum, Modern Operating Systems: Pearson New International Edition, Pearson Education, 2013 (Pearson Online) |
| R4 | Stallings, Operating Systems: Internals and Design Principles : International Edition, Pearson Education, 2013 (Pearson Online) |

**Modular Content Structure**

1. **Computer System Components and Interconnections**
   1. Organization and Architecture
   2. Structure and Functions of a computer system
   3. Computer Components
   4. Computer Functions
      1. Basic Instruction cycle state diagram
      2. Interrupts
      3. Instruction cycle state diagram with interrupts
      4. Interconnection Structures
      5. Bus Interconnection
   5. Performance Assessment
      1. MIPS Rate
      2. Amdahl’s Law
2. **Memory Organization**
   1. Computer Memory System Overview
      1. Characteristics of Memory Systems
      2. The Memory Hierarchy
   2. Cache Memory Principles
   3. Cache to Main Memory Mapping Functions: Direct, Associative, and Set Associative
   4. Replacement Algorithms
   5. Write Policy
   6. Multi-cache system
3. **Input/Output Organization**
   1. I/O Modules
   2. Data Transfer Schemes
      1. Programmed I/O
      2. Interrupt-Driven I/O
      3. Direct Memory Access
4. **Instruction Set Architecture (x86 as an example)**
   1. Instruction Set: Characteristics and Functions
      1. Machine Instruction Characteristics
      2. Types of Operands (Intel x86 Data Types as an example)
      3. Types of Operations (Intel x86 Operation Types as an example)
   2. Instruction Set: Addressing Modes and Formats
      1. Addressing Modes (x86 Addressing Modes as an example)
      2. Instruction Formats (x86 Instruction Formats as an example)

4.3 Instruction Pipeline

4.3.1 : Resource Hazard

4.3.2 : Data Hazard

4.3.3: Control Hazard

4.4 CISC Vs RISC

1. **Control Unit Operation**
   1. Hardwired Control Unit Implementation
   2. Micro programmed Control Unit Implementation
2. **Operating System Structure** 
   1. Introduction to Operating System
   2. Structure of a Operating System (Linux as an example OS)
   3. Operating System Services
   4. System Calls
3. **Process Management**
   1. Concept of Process
   2. Process State Diagram
   3. Operations on Processes
   4. Inter-process communications with examples
   5. Process vs. Threads
   6. Multithreading Models
   7. Process Scheduling criteria
   8. Process Scheduling Algorithms -FCFS, SJF, Priority, RR, Multilevel Queue, Multilevel Feedback Queue
4. **Process Coordination**
   1. The Critical section problem
   2. Peterson’s Solution
   3. Synchronization Hardware
   4. Semaphores
   5. Deadlock: System Model
   6. Deadlock Characterization
   7. Methods of Handling Deadlocks
      1. Deadlock Prevention
      2. Deadlock Avoidance: Banker’s Algorithm
      3. Deadlock Detection
      4. Recovery from Deadlock
5. **Memory Management**
   1. Memory-Management Strategies
   2. Swapping
   3. Contiguous memory Allocation
   4. Paging
   5. Segmentation
   6. Virtual-Memory Management
   7. Demand Paging
   8. Page Replacement Algorithms: FIFO, Optimal, LRU, LFU
   9. Thrashing
6. **File System**
   1. File Concept
   2. Access Methods
   3. Directory Structure
   4. File System Mounting
   5. File System Structure
   6. File System Implementation
   7. Directory Implementation

**Learning Outcomes:**

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| **No** | **Learning Outcomes** |
| LO1 | To **apply** the knowledge of performance metrics to find the performance of systems. |
| LO2 | To **Investigate** high performance architecture design |
| LO3 | To **Examine** different computer architectures and hardware |
| LO4 | Students will **Analyze and Compare** of process management concepts including scheduling, synchronization ,deadlocks |
| LO5 | Students will **Examine** multithreading and system resources sharing among the users |
| LO6 | Students will **Outline** of file system interface and implementation |

**Part B: Contact Session Plan**

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| **Academic Term** |  |
| **Course Title** | Computer Organization and Software Systems |
| **Course No** |  |
| **Lead Instructor** |  |

**Course Contents**

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| **Contact Hour** | **List of Topic Title**  **(from content structure in Part A)** | **Topic #**  **(from content structure in Part A)** | **Text/Ref Book/external resource** |
| 1-2 | **Computer System Components and Interconnections:**  Organization and Architecture, Structure and Functions of a computer system, Computer Components, Computer Functions: Basic Instruction cycle state diagram, Interrupts, Instruction cycle state diagram with interrupts. | 1.1-1.3, 1.4.1-1.4.3 | T1 |
| 2-4 | Interconnection Structures and Bus Interconnection  Performance Assessment : MIPS Rate, Amdahl’s Law  **Memory Organization :**  Computer Memory System Overview : Characteristics of Memory Systems and The Memory Hierarchy.  Cache Memory Principles. | 1.4.4-1.4.5, 1.5,2.1-2,2 | T1, R1 |
| 5-6 | Cache to Main Memory Mapping Functions: Direct, Associative, and Set Associative.  Replacement Algorithms, Write Policy, Multi-cache system. | 2.3-2.6 | T1 |
| 7-8 | **Input/Output Organization :**  I/O Modules, Data Transfer Schemes : Programmed I/O, Interrupt-Driven I/O, Direct Memory Access | 3.1-3.2 | T1 |
| 9-10 | **Instruction Set Architecture (x86 as an example):**  Instruction Set: Characteristics and Functions : Machine Instruction Characteristics, Types of Operands, Types of Operations,  Instruction Set: Addressing Modes and Formats: Addressing Modes, Instruction Formats | 4.1-4.2 | T1 |
| 11-12 | Instruction Pipeline :Resource Hazard, Data Hazard and Control Hazard | 4.3 | T1 |
| 13-14 | CISC Vs RISC.  **Control Unit Operation** : Hardwired Control Unit Implementation, Micro programmed Control Unit Implementation | 4.4, 5.1-5.2 | T1 |
| 15-16 | **Operating System Structure :** Introduction to Operating System, Structure of a Operating System (Linux as an example OS), Operating System Services , System Calls | 6.1-6.4 | T2 |
| 17-18 | **Process Management :** Concept of Process, Process State Diagram, Operations on Processes, Inter-process communications with examples, Process vs. Threads, Multithreading Models | 7.1-7.6 | T2 |
| 19-20 | Process Scheduling criteria, Process Scheduling Algorithms -FCFS, SJF, Priority, RR, Multilevel Queue, Multilevel Feedback Queue | 7.7-7.8 | T2 |
| 21-22 | **Process Coordination:** The Critical section problem, Peterson’s Solution, Synchronization Hardware | 8.1-8.3 | T2 |
| 23-24 | Semaphores.  Deadlock: System Model, Deadlock Characterization, Methods of Handling Deadlocks: Deadlock Prevention | 8.4-8.6, 8.7.1 | T2 |
| 25-26 | Deadlock Avoidance: Banker’s Algorithm, Deadlock Detection, Recovery from Deadlock | 8.7.2 – 8.7.4 | T2 |
| 27-28 | **Memory Management :** Memory-Management Strategies, Swapping, Contiguous memory Allocation, Paging, Segmentation | 9.1-9.5 | T2 |
| 29-30 | Virtual-Memory Management, Demand Paging, Page Replacement Algorithms: FIFO, Optimal, LRU, LFU  Thrashing. | 9.6 – 9.9 | T2 |
| 31-32 | **File System :** File Concept, Access Methods, Directory Structure, File System Mounting, File System Structure, File System Implementation, Directory Implementation | 10.1 – 10.7 | T2 |

**Evaluation Scheme**

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| **Evaluation Component** | **Name**  (Quiz, Lab, Project, Midterm exam, End semester exam, etc) | **Type**  (Open book, Closed book, Online, etc.) | **Weight** | **Duration** | **Day, Date, Session, Time** |
| **EC - 1** | Quizzes / Assignment |  | 30% |  | To be announced |
| **EC - 2** | Mid-term Exam | Closed book | 30% | 2 hours | To be announced |
| **EC - 3** | End Semester Exam | Open book | 40% | 3 hours | To be announced |

***Note*** *- Evaluation components can be tailored depending on the proposed model.*

**Important Information**

Syllabus for Mid-Semester Test (Closed Book): Topics in Weeks 1-8 (1-18 Hours)

Syllabus for Comprehensive Exam (Open Book): All topics given in plan of study

Evaluation Guidelines:

1. EC-1 consists of either two Assignments or three Quizzes. Announcements regarding the same will be made in a timely manner.
2. For Closed Book tests: No books or reference material of any kind will be permitted. Laptops/Mobiles of any kind are not allowed. Exchange of any material is not allowed.
3. For Open Book exams: Use of prescribed and reference text books, in original (not photocopies) is permitted. Class notes/slides as reference material in filed or bound form is permitted. However, loose sheets of paper will not be allowed. Use of calculators is permitted in all exams. Laptops/Mobiles of any kind are not allowed. Exchange of any material is not allowed.
4. If a student is unable to appear for the Regular Test/Exam due to genuine exigencies, the student should follow the procedure to apply for the Make-Up Test/Exam. The genuineness of the reason for absence in the Regular Exam shall be assessed prior to giving permission to appear for the Make-up Exam. Make-Up Test/Exam will be conducted only at selected exam centres on the dates to be announced later.

It shall be the responsibility of the individual student to be regular in maintaining the self-study schedule as given in the course handout, attend the lectures, and take all the prescribed evaluation components such as Assignment/Quiz, Mid-Semester Test and Comprehensive Exam according to the evaluation scheme provided in the handout.

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